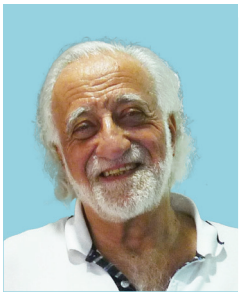
Citation

For pioneering and outstanding research in high-performance microprocessor architectures, especially involving instruction level parallelism, superscalar processor design, and high accuracy branch prediction



Dr. Yale N. Patt

Degree: PhD in Electrical Engineering, Stanford University, 1966

Date of Birth : June 29, 1939

Brief Biography :

1962 BSEE Northeastern University
1963 MS Electrical Engineering, Stanford University
1966 PhD Electrical Engineering, Stanford University
1966-1967
Assistant Professor, Electrical Engineering, Cornell University
1967-1969
United States Army Reserve
1969-1976
Associate Professor, Computer Science, NC State University
1976-1988
Professor of Mathematics and Computer Science, SF State University
1979-1988
Visiting Professor, EECS, UC Berkeley
1988-1999
Professor of EECS, University of Michigan, Ann Arbor
1999-2025
Ernest Cockrell, Jr. Centennial Chair in Engineering, UT Austin

Current Positions and Organization :

1999-present
Professor of Electrical and Computer Engineering, UT Austin
2011-present
University Distinguished Teaching Professor, UT Austin
2025-present
Virginia Cockrell Centennial Chair in Engineering, UT Austin

Main Awards and Honors :

1962 National Tau Beta Pi Fellow
1995 IEEE Emanuel R. Piore Medal
1996 IEEE/ACM Eckert-Mauchly Award
1999 IEEE Wallace W. McDowell Award
2000 ACM Karl V. Karlstrom Outstanding Educator Award
2005 IEEE Charles Babbage Award
2009 Honorary Doctorate, University of Belgrade
2011 IEEE B. Ramakrishna Rau Award (inaugural recipient)
2013 IEEE Harry H. Goode Award
2016 Benjamin Franklin Medal in Computer and Cognitive Sciences,from the Franklin Institute
2007-2024
Eight IEEE/ACM Test of Time Influential Paper Awards
2003-2011
Seven IEEE Micro Top Picks papers
1986-2012
Nine Conference Best Paper Awards
1986-2025
Invited Keynote address at 79 international conferences
1985-2019
Invited Lecturer at 77 University Distinguished Lecture Series
Fellow of the IEEE and ACM
Member of National Academy of Engineering (2014)

Main Achievements :

Yale Patt has amassed an outstanding record of both research and teaching during his 60 years as a professor.

Patt's pioneering research started with his WOS module while he was a graduate student in 1965. He realized that he could implement switching circuits with far fewer logical primitives and increased reliability over single transistor NAND gates in use at the time if he added at incremental cost more transistors to create the logical function performed by the primitive. As a result, he defined the WOS module, a very rich, complex, logically complete primitive as his basic building block, and published a paper at the 1967 Spring Joint Computer Conference.

Patt's most important research achievement came 20 years later with the invention of HPS, his high performance microarchitecture, research he did with three of his PhD students, Wen-mei Hwu, Stephen Melvin, and Michael Shebanow, and published as two papers in MICRO 1985.

HPS combined wide fetch and issue, decoding instructions into micro-ops, and out-of-order execution. Patt added result registers, which other researchers renamed a "reorder buffer" that allowed results to be temporarily stored so they could be retired in program order. In-order retirement guaranteed precise exceptions, retaining the integrity of the ISA.

Patt represented every instruction in a program as a data flow graph consisting of micro-ops. The data flow graph of each instruction was merged into the larger data flow graph consisting of all instructions that had previously been fetched but not yet retired. This established the core as a restricted data flow engine, restricted in the sense that the data flow graph consisted of only instructions that had been decoded and merged, but not yet retired.

Patt also added wide issue fetch and decode of instructions, increasing the rate of micro-ops supplied to the core. The data flow graph allowed the micro-ops themselves to control execution, eliminating the need for a complex but much less effective global controller.

Many dismissed HPS, stating that there was not enough parallelism to warrant the complexity of the engine, and there were not enough transistors available on the chip to implement it. Patt countered that data flow would provide the mechanisms for scheduling micro-ops, and Moore's Law would provide the transistors, which it did! Today, just about all high performance microprocessors embrace the path initiated by HPS.

However, HPS was not done. The microarchitecture was missing the ability to keep the processor core constantly supplied with enough micro-ops. That would require a very aggressive, highly accurate branch predictor -- which HPS did not yet have.

Patt and his student Tse-Yu Yeh proposed the Two level dynamic branch predictor in MICRO 1991. Branch prediction had been written off as a concept that would never make a big difference. The branch predictor of choice in 1991 was the saturating 2-bit counter, delivering accurate predictions 80% of the time. That meant taking the wrong path and recovering 20% of the time. The 2-bit counter based its predictions on the history of recent branches. Patt and Yeh claimed it wasn't the recent history but rather what the current branch did the last few times the history was the same as the current history of the branch being predicted. This change increased the prediction accuracy to 95%, decreasing the misprediction rate to 5%, an improvement of approximately 4x over the branch predictors in use at the time. Today, high accuracy branch predictors are an important part of every microprocessor, and follow the concepts introduced by Patt and Yeh.

Patt's research continues to be productive. He and his PhD students have continued to produce seminal research, among them the trace cache with Stephen Melvin (1989) and later with Sanjay Patel (1998), out-of-order fetch with Jared Stark (1999), run ahead execution with Onur Mutlu (2003), diverge-merge processors with Hyesoon Kim (2005), cache replacement with Moin Qureshi (2007), heterogenous processors with Aater Suleman (2010), Morphcore with Khubaib (2012), Tailored Page Sizes with Faruk Guvenilir (2019), Criticality driven fetch with Aniket Deshmukh (2023), and practical Ahead branch prediction with Chester Cai (2024).

For pioneering and outstanding research in high-performance microprocessor architectures, especially involving instruction level parallelism, superscalar processor design, and high accuracy branch prediction, Yale N. Patt is hereby awarded the Okawa Prize.